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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/062,503	02/05/2002	Hideki Murayama		4857
24956	7590	01/04/2005	EXAMINER	
MATTINGLY, STANGER & MALUR, P.C. 1800 DIAGONAL ROAD SUITE 370 ALEXANDRIA, VA 22314			THAI, TUAN V	
		ART UNIT		PAPER NUMBER
				2186

DATE MAILED: 01/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/062,503	MURAYAMA ET AL.
	Examiner Tuan V. Thai	Art Unit 2186

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 22 November 2004.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 21-46 is/are pending in the application.

4a) Of the above claim(s) 1-20 is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 21,22,24-28,30-33,38 and 41-46 is/are rejected.

7) Claim(s) 23,29,34-37,39 and 40 is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 05 February 2002 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

- Certified copies of the priority documents have been received.
- Certified copies of the priority documents have been received in Application No. 09/227,740.
- Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>11/30/20</u> .	6) <input type="checkbox"/> Other: _____

Part III DETAILED ACTION

Specification

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 28, 2004 has been entered.
2. Claims 21-46 are presented for examination. Claims 1-20 have been cancelled.
3. Applicant is reminded of the duty to fully disclose information under 37 CFR 1.56.

Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which

the invention was made.

5. Claims 21-22, 24-28, 30-33, 38 and 41-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ninomiya (USPN: 5,764,968);

As per claim 21; NiNomiya teaches the invention as claimed including a computer system (e.g. see figure 1, column 3, lines 35 et seq.) wherein a part of main memory is able to be hot plugged (e.g. card dock 40 which is an expansion unit of the computer main body can be hot inserted, e.g. see column 7, lines 36 et seq.), the computer system comprises a first memory is taught as memory 13 comprises system memory 131 mounted in advance on the system board, and an expanded memory 132 mounted by the user as needed (e.g. see figure 1, column 4, lines 22 et seq.); a nonvolatile storage storing configuration information regarding a second main memory to be hot plugged is taught as EEPROM 34 for storing information necessary for hot insertion, such as attributes of expansion cards mounted in the expansion slots of the docking station (addresses, DMA channels, IRQ numbers and the like) (e.g. see figure 2; column 7, lines 22 et seq.), a processor for acquiring the first and second memory information from the non-volatile storage and mapping the first memory based on the first and second memory information is taught as CPU 11 (figure 1) and/or control gate unit for accessing hot insertion information/data from the EEPROM 43 and known to

internally perform data mapping utilized first and second memory information from the EEPROM 43 under the control of the system BIOS when the computer main body and the card dock 40 are docked or when the computer main body or the card dock 40 is powered on (e.g. see column 7, lines 27-32; lines 48-53). Ninomiya, however does not particularly teach the processor unit accessing the non-volatile memory before initialization of an I/O device. First of all, it should be noted that Ninomiya clearly disclose the processor/ control gate unit 23 can access the EEPROM for hot insertion information as being detailed above (also see column 7, lines 27-32), EEPROM can further be accessed by different I/O units within the system for data updating/modification: Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention as made to allow the processor to access and read the hot insertion information, that known be stored in the EEPROM, prior to the initialization of the I/O device to allow the processor or gate control unit to complete its current operating tasks and saving critical operating data in lieu of after the initialization of the I/O device which results to occurrence of operation errors, therefore enhancing system reliability, and being greatly advantageous.

As per claim 22, wherein the processor generating first logical-physical address translating table for the first memory ... assigning a region to store a second logical-physical address

translating table for the second memory in the first memory is taught by Ninomiya to the extent that it is being claimed, since data being exchanged among memory 131 and modules on the docking station 30 (fig. 2), wherein table 1312b for storing system configuration information, and table 1312a for storing translated/driver programs, from which translation of addresses must occur for data mapping/matching (e.g. see column 4, lines 28-32);

As per claim 24, Ninomiya discloses table 1312a for storing translated/driver programs (e.g. see figure 1; column 4, lines 31-32); in addition, the CPU which utilized in the system of Ninomiya is implemented by a Pentium microprocessor from Intel which known to embed a translating table within itself for translating data as being claimed (e.g. see column 4, lines 16-17);

As per claim 25, Ninomiya clearly discloses the nonvolatile memory 34 is an EEPROM (e.g. see figure 2; column 7, lines 23 et seq.);

As per claim 26; NiNomiya teaches the invention as claimed including a computer system (e.g. see figure 1; column 3, lines 35 et seq.); a first memory is taught as memory 13 comprises system memory 131 mounted in advance on the system board, and an expanded memory 132 mounted by the user as needed (e.g. see figure 1, column 4, lines 22 et seq.); a nonvolatile storage storing configuration information regarding a second main memory

to be hot plugged is taught as EEPROM 34 for storing information necessary for hot insertion, such as attributes of expansion cards mounted in the expansion slots of the docking station (addresses, DMA channels, IRQ numbers and the like) (e.g. see figure 2; column 7, lines 22 et seq.); the processor acquiring the first and second memory information from the non-volatile storage and mapping the first memory based on the first and second memory information is taught as CPU 11 (figure 1) and/or control gate unit for accessing hot insertion information/data from the EEPROM 43 and known to internally perform mapping between first and second memory information under the control of the system BIOS when the computer main body and the card dock 40 are docked or when the computer main body or the card dock 40 is powered on (e.g. see column 7, lines 27-32; lines 48-53). Ninomiya, however does not particularly teach the processor unit accessing the non-volatile memory before initialization of an I/O device. First of all, it should be noted that Ninomiya clearly disclose the processor/ control gate unit 23 can access the EEPROM for hot insertion information as being detailed above (also see column 7, lines 27-32), EEPROM can further be accessed by different I/O units within the system for data updating/modification. Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention as made to allow the processor to access and read the hot insertion information, that known be stored in the EEPROM,

prior to the initialization of the I/O device to allow the processor or gate control unit to complete its current operating tasks and saving critical operating data in lieu of after the initialization of the I/O device which results to occurrence of operation errors, therefore enhancing system reliability, and being greatly advantageous.

As per claim 27, the further limitation of wherein the processor assigns a non-address translated region in the first main memory is equivalently taught as the used/unused RAS lines for unused/used banks prepared by the CPU 11 which associated with the system memory 131 (e.g. see column 9, lines 62 bridging column 10, line 9);

As per claim 28; Ninomiya discloses the system BIOS checks the size of banks connected to the RAS lines by write/read comparison or the like to detect unused banks (e.g. see column 10, lines 23 et seq.);

As per claim 30, Ninomiya discloses the non-address translated region being corresponded to the unused RAS lines for unused/used banks wherein the unused RAS lines are determined by the number of RAS lines prepared for the system memory 131 and the expanded memory 132 and the bank structure of the actually mounted memory module (e.g. see column 9, lines 29 bridging column 10, line 30);

As per claim 31, Ninomiya clearly discloses the nonvolatile memory 34 is an EEPROM (e.g. see figure 2; column 7, lines 23 et seq.);

As per claim 32, Ninomiya discloses table 1312a for storing translated/driver programs (e.g. see figure 1; column 4, lines 31-32); in addition, the CPU which utilized in the system of Ninomiya is implemented by a Pentium microprocessor from Intel which known to embed a translating table within itself for translating data as being claimed (e.g. see column 4, lines 16-17);

As per claim 33; NiNomiya teaches the invention as claimed including a computer system supporting a virtual memory system (e.g. see figure 1, column 3, lines 35 et seq.) comprising a first main memory is taught as memory 13 comprises system memory 131 mounted in advance on the system board, and an expanded memory 132 mounted by the user as needed (e.g. see figure 1, column 4, lines 22 et seq.); a nonvolatile storage storing configuration information regarding a second main memory to be hot plugged is taught as EEPROM 34 for storing information necessary for hot insertion, such as attributes of expansion cards mounted in the expansion slots of the docking station (addresses, DMA channels, IRQ numbers and the like) (e.g. see figure 2; column 7, lines 22 et seq.); the further limitation of the processor mapping the first main memory and acquiring said first information upon said mapping is taught as CPU 11 (figure

1) and/or control gate unit for accessing hot insertion information/data (first information) from the EEPROM 43 and known to internally perform data mapping on memory 13 utilized information from EEPROM 43 under the control of the system BIOS when the computer main body and the card dock 40 are docked or when the computer main body or the card dock 40 is powered on (e.g. see column 7, lines 27-32; lines 48-53). Ninomiya, however does not particularly teach the processor unit accessing the non-volatile memory before initialization of an I/O device. First of all, it should be noted that Ninomiya clearly disclose the processor/ control gate unit 23 can access the EEPROM for hot insertion information as being detailed above (also see column 7, lines 27-32), EEPROM can further be accessed by different I/O units within the system for data updating/modification. Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention as made to allow the processor to access and read the hot insertion information, that known be stored in the EEPROM, prior to the initialization of the I/O device to allow the processor or gate control unit to complete its current operating tasks and saving critical operating data in lieu of after the initialization of the I/O device which results to occurrence of operation errors, therefore enhancing system reliability, and being greatly advantageous.

As per claim 38, Ninomiya clearly discloses the nonvolatile memory 34 is an EEPROM (e.g. see figure 2; column 7, lines 23 et seq.);

As per claims 41, 43 and 45, the further limitation of wherein the non-volatile storage stores the second memory information preliminary before the second memory is hot-plugged is taught by Ninomiya; for example, Ninomiya clearly discloses that EEPROM 43 stores hot insertion information (information necessary for plug and play) such as the attributes of PC cards mounted in the expansion slots of the card dock 40. The hot insertion information is known to store within the EEPROM 43 before card dock 40 is mounted and said hot insertion information is read from the EEPROM 43 by the I/O control gate array 23 through the I2C bus 4 under the control of the system BIOS of the BIOS ROM 19 when the computer main body and the card dock 40 are docked (e.g. see column 7, lines 45-52).

As per claim 42, 44 and 46; Ninomiya further discloses wherein the non-volatile storage stores the first/second memory information when the computer main body or the card dock 40 is powered on (e.g. see column 7, lines 52-53).

Allowable subject matter

6. Claims 23, 29 and 34 are objected to as being dependent upon a rejected based claims, but would be allowable if rewritten in independent form including all of the limitations of the base

claim and any intervening claims. Claims 35-37 and 39-40 are also allowable since they are depended upon the indicated allowable claim 34.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

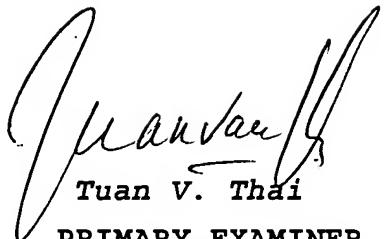
8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan V. Thai whose telephone number is (571)-272-4187. The examiner can normally be reached on from 6:30 A.M. to 4:00 P.M. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew M. Kim can be reached on (571)-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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TVT/December 16, 2004


Tuan V. Thai
PRIMARY EXAMINER
Group 2100